IN THE SPECIFICATION:

Please rewrite the paragraphs starting at page 2, line 23, and ending at page 3, line 13, as follows:

In the following the functions will be explained with reference to Fig. 2, which illustrates the potential states of the various areas. At a time t0, the transfer channel 5 is turned off and the photodiode area 2, 3 accumulates the photo-induced charge corresponding to the incident light amount. At a time t1, the transfer channel 5 is turned on to transfer the photo-induced charge to the CCD channel 6 through the transfer channel 5.

At times t2, t3, the control electrodes 8, 9 are controlled in succession to transfer the photo-induced charge is transferred in succession to the portions in the CCD channel 6, positioned directly below the control electrodes. The floating diffusion area 11 is reset in advance at the time t3, and, the photo-induced charge is transferred by the control electrode 10, at a time t4, to the floating diffusion area 11 and is converted therein into a voltage for output.

Please rewrite the paragraph starting at page 4, line 7, and ending at page 5, line 3, as follows:

Also, ~~the~~ Japanese Patent Application ~~Laid-open~~ Laid-Open No. 2-30189 discloses a configuration having an electrode for controlling the charge transfer from the photodiode to the CCD channel and another electrode for controlling the charge transfer in the CCD, as shown in Fig. 5. Referring to Fig. 5, a plurality of n-type accumulation areas 1 for accumulating the signal charges induced by the incident light are arranged on a p-type substrate 6, and a transfer gate ~~13~~ 3 is provided between the accumulation area 1 and a

A2

vertical CCD register 2, of which an end is connected to a horizontal CCD register composed of a transfer gate 12, a transfer electrode 13 for the vertical CCD register and a silicon dioxide layer 14. VA denotes the potential of the n-type accumulation area 1, taking the Fermi potential 15 of the interior of the p-type substrate as a reference, while VDEP denotes the potential VA required for completely depleting the accumulation area 1, and Vch denotes the channel potential when the transfer gate 3 is turned on. The potential VA is lowered in the drawing in response to the light entering the accumulation area 1, and the accumulated charge is transferred to the vertical CCD register 2 by lowering the potential of the gate 12.

Please rewrite the paragraph starting at page 5, line 10, and ending at page 6, line 9, as follows:

A3

In the field of solid state image pickup apparatus, in addition to the CCD, the MOS sensor is recently attracting attention and is being actively developed because of ~~the~~ advantages such as ease of one-chip formation of the peripheral circuits. For example, an exhibit titled "An Active Pixel Sensor Fabricated ~~Ysing~~ Using CMOS/CCD Process Technology" (exhibited at the 95 IEEE WORKSHOP on ~~Charge-coupled~~ Charge-Coupled Devices and Advanced Image Sensors) discloses a CMOS sensor and its potential chart as shown in Fig. 4. As shown in Fig. 4, in the CMOS sensor, the floating diffusion area 711 and the source follower amplifier (not shown) are provided for each pixel, instead of at the end of the CCD register in case of the CCD. In Fig. 4, components same as those in Fig. 1 are represented by same numbers. There are also shown a transfer gate 701 provided for each pixel, and a floating diffusion area 711 provided for each pixel. The photo-induced

A3

charge, generated in the photodiode area is transferred to the floating diffusion area 711, and the amplitude of the voltage generated therein according to amount of photo-induced charges is detected by the source follower amplifier, omitted in Fig. 4 but provided for each pixel, and outputted to an output line through a pixel selecting switch. There are also shown a reset gate 712 for resetting the floating diffusion area 711 provided for each pixel, and a reset drain 713 therefor.

Please rewrite the paragraph at page 6, lines 10-15, as follows:

A4

Such circuit configuration of transferring the charge of each pixel to the corresponding floating diffusion area 711 and effecting the selection of pixels by a common MOS circuit allows to achieve both a high S/N ratio as the sensor and a high performance realized by a one-chip MOS circuit.

Please rewrite the paragraph starting at page 10, line 18, and ending at page 11, line 5, as follows:

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Now, the function of the present embodiment will be explained with reference to Fig. 6B, showing the potential state of various areas at different timings. At a time t0, the transfer channel 5 is turned off and a photo-induced charge is accumulated in the photodiode area 2-4 according to the amount of ~~the~~ incident light. The floating diffusion area 11 is reset by turning on the reset gate 12 at a time t1. Then, at a time t2, the photo-induced charge is transferred from the photodiode area 2-4 through the transfer channel 5 to the floating diffusion area 11 and converted therein into a voltage and

A5

outputted. At a time t3, the transfer channel 5 is turned off again, and the photodiode area 2-4 of each pixel starts next charge accumulation.

Please rewrite the paragraphs starting at page 11, line 20, and ending at page 13, line 24, as follows:

A6

For explaining the circuit configuration of the solid state image pickup apparatus, an equivalent circuit corresponding to a pixel is shown in Fig. 8. A photodiode 101 accumulates a photo-induced charge which is transferred by a transfer switch 102, and the transferred photo-induced charge is temporarily stored in a floating diffusion area 103, amplified by a source follower MOS transistor 104 and is read out by a vertical selecting MOS transistor 105 to an output line 106. The floating diffusion area <u>103</u> is connected to a power source through a resetting MOS transistor 107, and, in the resetting operation by the application of a voltage of 5V to the gate thereof, the floating diffusion area <u>103</u> is reset to a potential of 5V-Vth.

For example, if the gate voltage of the resetting MOS transistor <u>102</u> is 5V for a power source voltage of 5V, the resetting voltage becomes 5V-Vth. The threshold voltage of the MOS transistor cannot be made completely free from fluctuation because of fluctuation in the fluctuation of the Si layer or in the thickness of the gate insulation layer, so that the resetting voltage inevitably shows a fluctuation.

Also, with an increase in the threshold value Vth, the effective resetting voltage is lowered so that the potential well becomes shallower as shown in t2' in Fig. 7A. In such state, if the gate voltage and the threshold voltage of the transferring MOS transistor <u>102</u> remain constant, there will result charge remaining in the channel of the

transferring MOS transistor 102 as shown in t2'. In order to prevent such charge remaining phenomenon, it is effective to lower the gate voltage of the transferring MOS transistor 102 as shown in t2". Consequently the voltage of the gate 501 of the transferring MOS transistor 102 is controlled by the first potential setting circuit 502, independently from the voltage of the gate 12 of the resetting MOS transistor 107. Also, in order to shift from the state shown in t2' in Fig. 7A to the state shown in t2", the voltage of the gate 501 of the transferring MOS transistor 102 is lowered to reduce the potential of the channel 5 thereof, thereby transferring the charge in the channel to the floating diffusion area 103.

A2

More specifically, in a case of the electron accumulation type as shown in Fig. 7B, for example when a gate-on voltage is 5 V for the resetting MOS transistor 107, a reset voltage is 3.5V = 5V-Vth (Vth = 1.5V) for the floating diffusion area 103, a saturation signal voltage is 1.5V, a saturation voltage is 2V for the floating diffusion area 103 and a depletion voltage is 1V for the photodiode, the gate-on voltage Vg of the transferring MOS transistor 102 is so set as to satisfy a relation 1 + Vth' < Vg < 2 + Vth' (for example, 2.5 V < Vg < 3.5V). As an example, Vg is selected as 3.3V.

If the resetting voltage varies from 3.5 V to 3.2 V by the fluctuation of the process, the saturation voltage at the floating diffusion area 103 becomes 1.7 V, so that the charge remains in the channel of the transferring MOS transistor 102 unless Vg is so selected as to satisfy a condition 2.5V < Vg < 3.2V.

Please rewrite the paragraph starting at page 14, line 26, and ending at page 15, line 25, as follows:

There are also shown a voltage supply unit 113 such as a battery, a voltage conversion circuit 114 for converting the voltage of the voltage supply unit 114 into a desired voltage, variable resistors 115, 116, a power supply voltage input terminal 112 for entering a voltage for driving the solid state image pickup apparatus, and an input terminal 111 for entering a voltage for driving the transferring MOS transistor 102. In addition, there are shown signal lines 105', 102' and 107' for respectively supplying pulses ϕ_{SEL}, ϕ_{TX} and ϕ_{RES} to be used to turn on and off the vertical selecting MOS transistor 105, the transfer switch 102 and the resetting MOS transistor 107. Under a condition that a pulse is applied from the vertical shift register 108 to one of input terminals of each of the three AND circuits, the AND circuit 109 outputs the voltage value input from the terminal 112, when the pulse ϕ_{SEL} is applied to the signal line 105'; the AND circuit 109' outputs the voltage value input from the terminal 111, when the pulse ϕ_{TX} is applied to the signal line 102'; and the AND circuit 109" outputs-the voltage value input from the terminal 112, when the pulse ϕ_{RES} is applied to the signal line 107'. In the present embodiment, the AND circuit 109, the input terminal 111 and the variable resistor 116 constitute the first voltage setting circuit 502 shown in Figs. 6A and 6B.

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Please rewrite the paragraph at page 16, lines 5-18, as follows:

As the voltage ~~entered from~~ at the input terminal 111 can be made different, by the variable resistor 116, from the voltage ~~entered from~~ at the power supply voltage input terminal 112, the potential well can be realized in a form ~~as~~ shown by t2" in Fig. 7A by reducing the voltage entered from the input terminal 111. Thus, in the present embodiment, the pulse voltage for driving the transferring MOS transistor 102 can be

A8

adjusted independently from the pulse voltage for driving the resetting MOS transistor 107. Consequently, even if the resetting voltage is lowered by the fluctuation in the manufacturing process, the ideal potential well can be formed by adjusting the pulse for driving the transferring MOS transistor 102.

A8

Please rewrite the paragraph starting at page 16, line 26, and ending at page 17, line 10, as follows:

Fig. 10 is a view showing the potentials of various areas for explaining a second embodiment of the present invention. In contrast to the first embodiment, in which the proper transferring operation is realized, even in the presence of fluctuation in the manufacturing process, by controlling the voltage of the transferring MOS transistor 102, the present embodiment is to achieve a similar effect by controlling the voltage of the resetting MOS transistor 102. The circuit configuration corresponding to Fig. 10 is similar to that shown in Figs. 6A and 6B and will not, therefore, be explained further.

A9

Please rewrite the paragraph at page 18, lines 3-17, as follows:

As the voltage ~~entered from~~ at the input terminal 111 can be made different, by the variable resistor, from the voltage ~~entered from~~ at the power supply voltage input terminal 112, the potential well can be realized in a form as shown by t2" in Fig. 10 by elevating the voltage entered from the input terminal 111. Thus, in the present embodiment, the pulse voltage for driving the resetting MOS transistor 107 can be adjusted independently from the pulse voltage for driving the transferring MOS transistor 102. Consequently, even if the potential of the floating diffusion area 103 comes close to that of

A10

the transferring MOS transistor 102 by the fluctuation in the manufacturing process, the ideal potential well can be formed by adjusting the pulse for driving the resetting MOS transistor 107.

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Please rewrite the paragraph starting at page 18, line 22, and ending at page 19, line 18, as follows:

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As shown at a time t2' in Fig. 10, the resetting voltage may vary for example because of fluctuation in the manufacturing process, resulting in a charge remaining in the transfer channel 5. In the present embodiment, however, the voltage of the reset gate 12 is independently controlled by the second potential setting circuit 503 for elevating the resetting voltage of the floating diffusion area 11. For example, if the resetting voltage varies from 3.5 V to 3.3 V in the example shown in Fig. 7B, it can be returned to 3.5 V by varying the gate-on voltage of the resetting MOS transistor 107. In this manner, the proper transferring operation can be realized without changing the conditions of the transferring MOS transistor 102. Such setting realizes a condition:

saturation voltage of floating diffusion area 11 >
channel voltage of transfer MOS transistor in
on-state > depletion voltage of photodiode,

whereby the charge can be transferred to the floating diffusion area 103 without remaining on the photodiode and the channel of the transferring MOS transistor 102, and there can be achieved an effect similar to that of the first embodiment for preventing the charge remaining in the transfer channel 5.

Please rewrite the paragraph at page 20, lines 12-20, as follows:

A12

The circuit shown in Fig. 13 is so designed as ~~to~~ independently to set the power supply voltage for driving the solid state image pickup apparatus, the voltage supplied to the gate of the transferring MOS transistor 102 and the voltage supplied to the gate of the resetting MOS transistor 107, but the voltage supplied to the gate of the transferring MOS transistor 102 or that supplied to the gate of the resetting MOS transistor 107 may be made common with the power supply voltage. In Fig. 13, the first and second potential setting circuits are constituted by the AND circuit 109 and a voltage adjusting circuit.